3.1.1.5 Real Time Clock

A serial access clock chip (U8) provides a real time clock and calendar, as well as several bytes of non-volatile RAM for use by the microcontroller. The data in the chip is maintained in the absence of +5V-STBY power using a 3V lithium battery (B1). The RAM in the clock chip stores user-set communication parameters (RS-232 baud rate, etc) for access by the microcontroller when the projector is off.

3.1.2 68000 Microprocessor

The 68000 utilizes a 16-bit external data bus (D0-D15) and a 23-bit address bus. Only the first 19 address bits (A1-A19), defining a megabyte of address space, are used on the Control Board. This address space is decoded into several smaller ranges by ICs U28 and U30, which generate chip selects for all of the major circuits on the Control Board. (Refer to Appendix B for details of the address map.) ICs U1, U23, U24, U25 and U26 buffer the address, data and bus control signals for distribution off-board to the projector's expansion slots.

Power-on reset of the 68000 is handled by the microcontroller. When it asserts PWR-EN* low to turn on the power supplies, it also pulls RESET* low to hold the 68000 microprocessor in a reset state. When the supply voltages have stabilized, RESET* is pulled high and the microprocessor begins operation.

3.1.2.1 Memory

The projector's system software resides in a 16-bit EPROM (U35). Memory for stack space, variables and the projector's setup database is provided by two static RAMs (U31, U32). The content of the RAM chips is maintained in the absence of power using the 3V lithium battery (B1). The micromanager IC (U17) switches automatically to the battery when the +5V-STBY rail disappears, ensuring a continuous supply voltage (VBAT) to the RAM chips (and to clock chip U8). The micromanager IC also write-protects the RAM when switching to the battery. It accepts the chip select CS-RAM* and conditions it to produce CSTORAM*.

All data transfers by the 68000 are zero wait state, except those involving the Character Generator. Read or write access to the Character Generator during the visible portion of a video scan line results in the insertion of wait states, which delay the assertion of DTACK* from PAL U28 until a horizontal or vertical blanking interval occurs. This eliminates visible glitching of the on-screen image. Refer to section 3.1.2 of the Character Generator description for further details.

3.1.2.2 Interrupts

There are five interrupts sources; V-DRIVE, DPB-I, IOP-I, ACON-I, and TIMER (listed in order of decreasing priority). The V-DRIVE interrupt is created on the leading edge of the vertical drive pulse from the DPB. It marks the start of the vertical flyback interval. V-DRIVE is normally non-maskable, but becomes disabled when the NO-NMI signal from the microcontroller is driven high. The DPB-I, IOP-I, and ACON-I interrupts occur when one of the microcontrollers on the Control Board, DPB or expansion slot, respectively, communicates with the 68000. The TIMER interrupt is a periodic pulse from the microcontroller which is used as a time reference by the software.